The Endurance Performance of 0.5µm FRAM Products

Authors: Fan Chu and Tom Davenport

INTRODUCTION

Ferroelectric random access memories (FRAMs) are nonvolatile memory devices that store data by using the bi-stable switchable polarization state of a ferroelectric material. Ferroelectric thin films exhibit the hysteresis effect of polarization versus applied electrical field (P-E hysteresis loop) to realize its nonvolatile storage capability. FRAM is also known for its high endurance, a fast write speed, and low power consumption. Endurance is defined as the ability of the device to sustain switchable polarization after many switching cycles. It is one of the critical performance characteristics for FRAM applications. Due to the high endurance of FRAM devices, evaluating the endurance behavior in a reasonable amount of time becomes difficult. Table 1 shows the time needed to exercise a 64Kb parallel FRAM device at number of cycles at various cycling frequencies. It can be seen that at 5 MHz, it will take about six months to reach 10^{10} endurance cycles. Even at 10MHz, it will still take more than three months to reach 10^{10} cycles.

Table 1. Number of Days to Exercise a 64Kb parallel FRAM Device

Cycling Freq.	Number of Endurance Cycles		
	10^8	10^9	10^{10}
1MHz	9.50	95.0	950
5MHz	1.90	19.0	190
10MHz	0.95	9.5	95

HIGHER VOLTAGE REDUCES TEST TIME

In order to evaluate the endurance behavior of
FRAM products within a reasonably short period of time, we need to speed up the polarization fatigue process or reduce the number of endurance cycles using certain measures. An effective way to do this is to utilize high voltage acceleration. Figure 1 demonstrates that applying voltages higher than the operating voltage of the part can indeed accelerate fatigue processes and consequently reduce the endurance test time.

This paper will use an endurance model to predict the endurance performance using a high voltage acceleration approach.

EXPERIMENTAL METHOD

The samples used in this experiment are 50 x 50 µm ferroelectric capacitors and array structures on product wafers. Each array structure contains 1200 small capacitors.

Q_{SW} Measurement: Conventional dynamic P-E hysteresis loop measurements do not accurately reflect the real operation of the FRAM device. The switching performance of ferroelectric thin films is instead characterized using a four-pulse sequence called the positive-up, negative-down (PUND) approach that closely mimics the FRAM device operation. Figure 2 shows a typical pulse train of this four-pulse approach and corresponding response as a hysteresis loop. The switched charge density, Q_{SW} (which equals approximately $2*P_R$ defined below), reflects the switching behavior of ferroelectric thin films using the four-pulse sequence method. Q_{SW} vs. applied voltage describes the switching behavior of ferroelectric thin film capacitors. Figure 2 shows a typical Q_{SW} as a function of applied voltage, in which:

$$Q_{SW} = \{(N-D) + (P-U)\}/2 \approx 2*P_R \qquad Eq.\ 1$$

P_R is the remanent polarization that can be obtained from a conventional hysteresis loop measurement. Q_{SW} is called switched charge (or more strictly, switched charge density). Q_{SW} is the sum of polarizations generated from the ferroelectric domains that are re-oriented along the direction of applied electric field.

Endurance Measurement: The endurance was tested using a pulse sequence as shown in Figure 3. The ferroelectric capacitor array was exercised at a continuous rate of 3.3MHz.

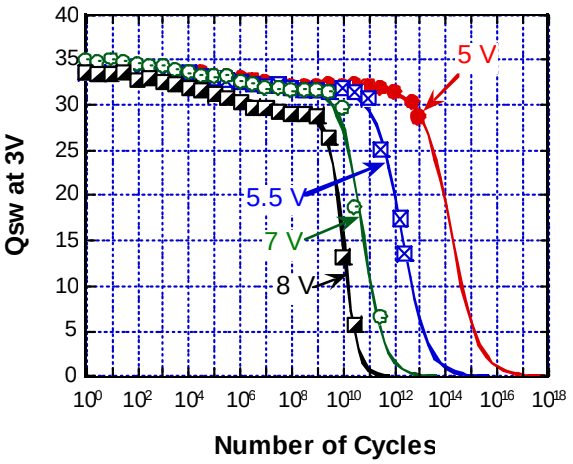

Figure 1. Q_{SW} vs. Endurance Cycles shows fatigue is accelerated at higher applied voltages

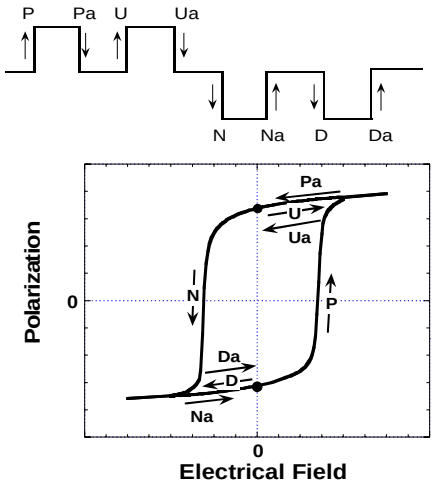

Figure 2. Pulse Train and Corresponding Hysteresis Loop

THE ENDURANCE MODEL

The endurance model used in this paper is shown in Eq.2:

$$Q_{SW}(N) = (Qi + k\ logN) / [1 + (N / N_0)^{1/S}] \qquad Eq.2$$

where N is the number of endurance cycles, N_0 is the number of endurance cycles at which 50% of ferroelectric domains are pinned, Qi is the initial switched charge, S is a

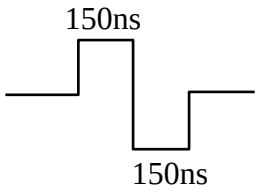

Figure 3. Endurance Test

shape factor that determines the shape of distribution, and *k* is the slope of the linear Q_{SW} increase or decrease as a function of *log N*.

Figure 4 shows the fitting result using *Eq. 2* for ferroelectric array capacitors. It can be seen that the endurance model (*Eq. 2*) fits the experimental data very well, suggesting the model can precisely describe the endurance performance.

By applying the endurance model to the endurance curves, the parameter *Qi*, N_0, *S* and *k* as a function of voltage can be obtained. Those correlations can be fitted to the simplest function under two boundary conditions, i.e. 1) with sufficiently high voltage, all the fatigue mechanisms are activated, and continuing to increase the voltage will not activate more fatigue process, and 2) when the applied voltage is close to zero, there should be no concern of fatigue as the switching is close to zero. High voltage (6.5V) was applied on the capacitor in order to speed the fatigue process and check the validity of the model.

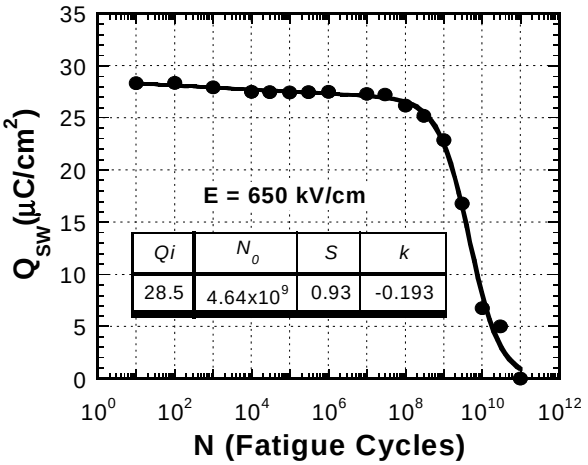

Figure 4. Q_{SW} vs. Number of Fatigue Cycles Shows Excellent Fit

The N_0, *S, and k* values under nominal voltages, such as 3.3V, can be obtained by extrapolating N_0, *S* and *k* as a function of voltage to 3.3V. The *Qi* value can be obtained from standard Q_{SW} vs. the applied test voltage. Combining Eq. 2 and nominal voltage values for N_0, *S*, *k* and *Qi*, the endurance performance of the investigated materials under operating voltage conditions can be predicted. Figure 5 shows the predicted 3.3V endurance performance of the integrated ferroelectric capacitor array processed using 0.5µm process.

It can be seen that for the ferroelectric capacitor arrays built on a 0.5µm process, after 10^{16} 3.3V endurance cycles (Figure 5), there will be about 10 µC/cm^2 switchable charge left, which is more than the minimum sensing level of 6 µC/cm^2. Therefore 0.5µm 3.3V FRAM products are expected to pass the standard QA tests after being exercised at 3.3V for at least 10^{16} cycles.

CONCLUSION

The endurance performance of FRAM is characterized by a mathematical model which predicts that a 1.0 x 10^{16} specification is appropriate.

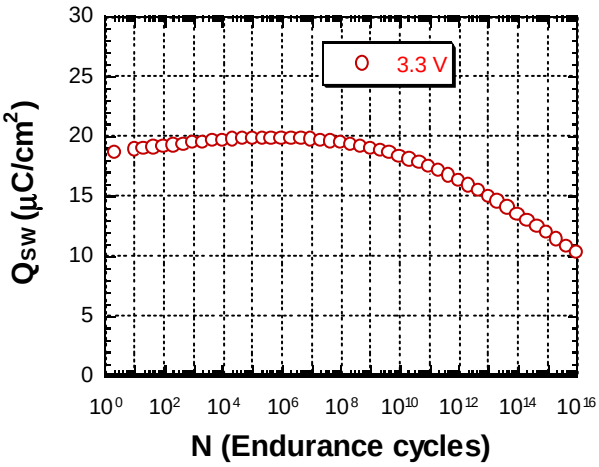

Figure 5. Predicted Endurance Performance for the 0.5 µm Process at 3.3V